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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,115	10/21/2003	Paul Andrys	SK00002C1 (00CXT0656C1)	5326

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Francisco A. Rubio-Campos
Suite B-104
26895 Aliso Creek Road
Aliso Viejo, CA 92656-5301

EXAMINER	
NGUYEN, KHANH V	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,115	ANDRYS ET AL.	
	Examiner	Art Unit	
	Khanh V. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-5, 8-15, 18-25, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Jarvinen (6,052,032).

Regarding claims 1, 11, Jarvinen (Figs 1-3) discloses an amplifier circuit comprising: a resistors (not label); and a bias voltage input terminal (V_{bias}) for receiving bias voltage connected to the resistor (not label) resulting a bias current via the resistor, wherein the bias voltage is always present.in the reference circuit and the resistor (not

label) is a resistor connected between the base of transistor (Q2) and the bias voltage (Vbias).

Regarding claims 2, 12, wherein diode connected transistor (Q3, Q4) of Fig. 2 are capable of performing the function of clamp circuit.

Regarding claims 3, 13, the bias current of the reference circuit is in a linear relationship with the bias voltage (Vbias).

Regarding claims 4, 14, wherein plurality of components in the reference circuit are inherently seen connected to resistor (not label).

Regarding claims 5, 15, 25, wherein the components and the resistor having different characteristics and they are inherently seen having substrate.

Regarding claims 8, 18, wherein the reference circuit discloses a single stage amplifier circuit.

Regarding claims 9, 19, wherein Fig. 3 discloses a multi-stage amplifier.

Regarding claims 10, 20, 27, wherein Fig. 3 discloses transistors (Q2, Qc, Qd2) and resistor (Rbm) connected in a feedback loop having the function thereof.

Regarding claims 22, 23, the methods recited are inherent to the operation of the reference circuit since the diode/diode connected transistor (26, 26a) can be clamped to a value that is above the predetermined threshold.

Regarding claim 24, wherein the bias current and a current between the Vsup and the base of transistor (Q1) called Ibase are mirror since they are connected in parallel

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6, 7, 16, 17, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarvinen.

Jarvinen discloses the claimed invention except the type of transistor used. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the transistors of the reference circuit with CMOS or Gallium Arsenide Semiconductor, since applicant has not disclosed that CMOS or Gallium Arsenide Semiconductor solves any particular problem or is for any particular purpose and in light of any criticality or unexpected result it appears that the invention would perform equally well with CMOS or Gallium Arsenide Semiconductor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional references (Poulin (et al. (6,304,130); Apel (6,441,687); Morizuka (6,448,859)) disclose amplifier circuit having bias voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHANH VAN NGUYEN
PRIMARY EXAMINER
Art Unit: 2817